Claims

[c1] An integrated circuit comprising:

at least one memory cell pair having first and second memory cells arranged in a memory group, a memory cell includes a cell transistor having first and second diffusion regions and a cell capacitor having a dielectric layer between first and second electrodes, wherein the cell transistors of the memory cell pair share a common second diffusion region;

a first bottom electrode plug coupling the first electrode of the first memory cell capacitor to the common second diffusion region;

a second bottom electrode plug coupling the first electrode of the second memory cell capacitor to the common second diffusion region; and

the second electrode of the first memory cell capacitor is coupled to the first diffusion region of the first memory cell transistor and the second electrode of the second memory cell capacitor is coupled to the first diffusion region of the second cell transistor.

[c2] The integrated circuit of claim 1 wherein the memory cells are ferroelectric memory cells.

[c3] The integrated circuit of claim 2 wherein the memory group comprises 2^{y} memory cells.

[c4] The integrated circuit of claim 2 further comprises at least 1 additional memory cell pair, wherein adjacent cell transistors of two adjacent memory cell pairs share a common first diffusion region and second electrodes of capacitors of adjacent memory cell pairs are commonly coupled to the common first diffusion region.

[c5] The integrated circuit of claim 4 wherein the memory group comprises 2^{y} memory cells.

[c6] The integrated circuit of claim 1 further comprises at least 1 additional memory cell pair, wherein adjacent cell transistors of two adjacent memory cell pairs share a common first diffusion region and second electrodes of capacitors of adjacent memory cell pairs are commonly coupled to the common first diffusion

region.

[c7] The integrated circuit of claim 6 wherein the memory group comprises 2^y memory cells.

[c8] The integrated circuit of claim 1 wherein the memory group comprises 2^y memory cells.

[c9] The integrated circuit of claim 1 wherein the cell capacitor further comprises a barrier layer between the first electrode and bottom electrode plug.

[c10] 10.The integrated circuit of claim 9 wherein the capacitors of the memory cells are formed in a single etch step.

[c11] The integrated circuit of claim 10 wherein the cell capacitors of one memory cell pair share a common first electrode.

[c12] The integrated circuit of claim 10 wherein the cell capacitors of one memory cell pair share a common barrier layer.

[c13] The integrated circuit of claim 12 wherein the cell capacitors of one memory cell pair share a common first electrode.

[c14] An integrated circuit comprising:
at least one memory cell pair having first and second memory cells arranged in a memory group, a memory cell includes a cell transistor having first and second diffusion regions and a cell capacitor having a dielectric layer between first and second electrodes, wherein the cell transistors of the memory cell pair share a common second diffusion region;
a bottom electrode plug coupling the first electrodes of the capacitors of the memory cell pair to the common second diffusion region, the bottom electrode plug sufficiently large to provide sufficient overlap to the first electrodes; and
the second electrodes of the capacitors coupled to first diffusion regions of respective cell transistors.